A method for manufacturing a power transistor circuit includes securing a die to a substrate, the die comprising a transistor having an input terminal and an output terminal. One or more performance characteristics of the transistor are measured. Using one or more wire sets, the transistor input terminal is electrically connected to one or more input matching elements and an input signal lead. The impedance of the one or more wire sets, as determined by selecting a desired number and/or length of the wires in each set, is selected based at least in part on the measured transistor performance characteristic(s). Similarly, using one or more additional wire sets, the transistor output terminal is electrically connected to one or more output matching elements and an output signal lead, wherein the impedance of the additional wire sets is selected based at least in part on the measured transistor performance characteristic(s).

Remarks

The error in line 6 of the abstract has been corrected. A marked-up version of the amended abstract is attached hereto.

Claims 1-16 stand rejected under 35 U.S.C. § 103(a) over USP 5,371,405 ("Kagawa") in view of JP404048756A ("Nishiuma"). Of these claims, 1, 5, 9 and13 are independent. For the following reasons, Applicants request reconsideration and withdrawal of the claim rejections under § 103.